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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,403	01/09/2004	Takumi Yamaguchi	10873.1377US01	7971
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EXAMINER PETERSON, CHRISTOPHER K				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/754,403

Applicant(s)

YAMAGUCHI ET AL.

Examiner

CHRISTOPHER K. PETERSON

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. The Amendment After Non-Final Rejection filed on 8/28/2008 has been received and made of record. Examiner notes that the Applicant has amended claims 1 and 2. Claims 1 - 22 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 2 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1 – 5, 9-14 and 16- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (US Patent # 6,593,562) in view of Voss (US Patent # 7,233,354).**

As to claim 1, Parrish (Fig. 8) teaches a solid-state imaging, device, comprising:

- an imaging region (array 60) in which a plurality of pixels (detector pixels 62-1 – 62-N) are arranged (Col. 8, lines 8 – 24). Parrish teaches the array (60) may be, for example, a linear array of detector elements or a two dimensional array of detector elements (Col. 8, lines 11 – 13).

- a signal line (output of the output amplifier 102) through which a pixel signal of the imaging region (60) is read out (Col. 11, lines 1 - 14). Parrish teaches the output amplifier 102 to, for example, an external system in which electro-optical sensor 58 is employed.
- wherein a plurality of adding circuits (read-out integrated circuit (ROIC) 64) for adding pixel signal charges obtained from two or more of the pixels (62-1 - 62-N) is provided so that an output signal of each adding circuit is read out to the signal line (100), each adding circuit comprising an adding portion (sub-pixel switches 68-1 - 68-N), a gain control portion (integrating amplifiers 94-1 - 94-N) and a storage portion (sample and hold circuit 108-1), so that an output signal of the adding portion is subjected to a gain control by the gain control portion and then stored in the storage portion (Col 8 lines 25 - 36 and Col. 11, lines 34 - 65). Parrish teaches each set of sub-pixel switches is electrically coupled to the sub-pixel detector elements of a corresponding detector pixel and to the input of a corresponding one of gain chains 70-1-70-N and a sub-pixel selection logic (72) controls the sub-pixel switches (Col 8 lines 25 - 36).

Parrish (Fig. 20) teaches the detector elements by selecting a plurality of sub-pixel switches combinations and testing the performance of each combination (Col. 14, lines 6 - 56). Parrish does not specifically teach controlling the gain of the integrating amplifiers (94-1 - 94-N). Voss reference teaches wherein on the basis of a predetermined reference quantity of light (light-level sensor 55) incident onto the

imaging region (24), a gain of the adding circuit in a condition in which a quantity of the incident light is above the reference quantity is controlled to be smaller than a gain of the adding circuit in a condition in which a quantity of the incident light is below the reference quantity (Col. 5 line 54 – Col.6, line 4). Voss teaches the microprocessor decides to adjust the gain, resolution, or both depending on the light-level sensor (55). The microprocessor would provide a small gain when in the incident light is high and provide a large gain for low incident light (Col. 5 line 62 – Col.6, line 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided gain control circuit as taught by Voss to the read-out integrated circuit (ROIC) of Parrish, to reduce blur and noise problems and provide a user with readily accessible independent and dynamic range control of the resolution and light gathering ability of the image capturing medium (Col. 2, lines 7 – 22 of Voss).

As to claim 2, Parrish (Fig. 8) teaches a solid-state imaging device, comprising:

- an imaging region (array 60) in which a plurality of pixels (detector pixels 62-1 – 62-N) are arranged (Col. 8, lines 8 – 24). Parrish teaches the array (60) may be, for example, a linear array of detector elements or a two dimensional array of detector elements (Col. 8, lines 11 – 13).
- a signal line (output of the output amplifier 102) through which a pixel signal of the imaging region (60) is read out (Col. 11, lines 1 - 14). Parrish teaches the output amplifier 102 to, for example, an external system in which electro-optical sensor 58 is employed.

- wherein a plurality of adding circuits (read-out integrated circuit (ROIC) 64) for adding pixel signal charges obtained from two or more of the pixels (62-1 – 62-N) is provided so that an output signal of each adding circuit is read out to the signal line (100), each adding circuit comprising an adding portion (sub-pixel switches 68-1 - 68-N), a gain control portion (integrating amplifiers 94-1 - 94-N) and a storage portion (sample and hold circuit 108-1), so that an output signal of the adding portion is subjected to a gain control by the gain control portion and then stored in the storage portion (Col 8 lines 25 – 36 and Col. 11, lines 34 - 65). Parrish teaches each set of sub-pixel switches is electrically coupled to the sub-pixel detector elements of a corresponding detector pixel and to the input of a corresponding one of signal chains 70-1-70-N and a sub-pixel selection logic (72) controls the sub-pixel switches (Col 8 lines 25 – 36).

Parrish (Fig. 20) teaches the detector elements by selecting a plurality of sub-pixel switches combinations and testing the performance of each combination (Col. 14, lines 6 – 56). Parrish does not specifically teach controlling the gain of the integrating amplifiers (94-1 - 94-N). Voss reference teaches wherein within at least a partial range of a quantity of incident light onto the imaging region (24), a gain of the adding circuit is controlled to decrease with an increase of the quantity of the incident light (Col. 5 line 54 – Col.6, line 4). Voss teaches the microprocessor decides to adjust the gain, resolution, or both depending on the light-level sensor (55). The microprocessor would provide a small gain when in the incident light is high and provide a large gain for low incident light

(Col. 5 line 62 – Col.6, line 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided gain control circuit as taught by Voss to the read-out integrated circuit (ROIC) of Parrish, to reduce blur and noise problems and provide a user with readily accessible independent and dynamic range control of the resolution and light gathering ability of the image capturing medium (Col. 2, lines 7 – 22 of Voss).

As to claim 3, Parrish teaches wherein the adding circuit (64) is arranged between the imaging region (60) and the signal line (output of the output amplifier 102) (Col. 11, lines 1 - 14).

As to claim 4, Parrish teaches wherein a plurality of the adding circuits (68-1 – 68-N) are arranged between the two or more pixels (62-1 – 62_N) included in the respective sets of pixels (Col. 8, lines 8 – 24). The sub-pixel switches must be between the detector pixels for the sub-pixel switches to combine the detector pixel values.

As to claim 5, Voss teaches the solid-state imaging device according to claim 1, wherein a plurality of the adding circuits are provided, and gains for at least two of the plurality of adding circuits are controlled individually (Col.6., line 50 – 67). Voss teaches the summing function occurs before any gain is applied to the signal (Col. 6, line 59 – 64). This increases the signal to noise ratio.

As to claim 9, Voss teaches wherein when signals of N pieces of pixels (added pixels) are added, a gain of the adding circuit (24, 26, 28, 32 and 38) is controlled so that an output value from the adding circuit is not more than a value obtained from the following formula: (value obtained by adding the N pieces of signals) / N (Col. 5 line 62

– Col.6, line 4). Voss teaches the microprocessor decides to adjust the gain, resolution, or both depending on the light-level sensor (55). The microprocessor would provide a small gain when in the incident light is high and provide a large gain for low incident light (Col. 5 line 62 – Col.6, line 4).

As to claim 10, Voss teaches wherein when signals of N pieces of pixels are added, a gain of the adding circuit (24, 26, 28, 32 and 38) is controlled so that an output value from the adding circuit is less than a value obtained by adding the N pieces of signals and more than a value obtained from the following formula: (value obtained by adding the N pieces of signals) / N (Col. 5 line 62 – Col.6, line 4). Voss teaches the microprocessor decides to adjust the gain, resolution, or both depending on the light-level sensor (55). The microprocessor would provide a small gain when in the incident light is high and provide a large gain for low incident light (Col. 5 line 62 – Col.6, line 4).

As to claim 11, Voss teaches a camera (10) equipped with the solid-state imaging device according to claim 1 (Col. 3, lines 42 – 51).

As to claim 19, Voss teaches wherein a gain (26) is controlled for each of the plurality of signals (Col. 5, line 54 – Col. 6, line 4). Voss teaches the microprocessor (32) decides if the gain is used or change in resolution.

As to claims 12 - 14, 16 - 18 and 20, these claims differ from claims 1, 3, 4, 5 - 7, 9 - 11 and 19 only in that the claims 12 - 14, 16 - 18 and 20 depend on claim 2 and claims 1, 3, 4, 5 - 7, 9 - 11 and 19 depend on claim 1. Thus claims 12 - 14, 16 - 18 and 20 are analyzed as previously discussed with respect to claims 1, 3, 4, 5 - 7, 9 - 11 and 19 above.

5. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (US Patent # 6,593,562) in view of Voss (US Patent # 7,233,354) , and further in view of Fossum (US Patent # 5,949,483).

As to claim 8, note the discussion above. Voss does not teach an adding circuit is provided with an averaging portion. Fossum (Fig. 7 and 8) teaches an averaging portion (608 and 610) for averaging pixel signals obtained from two or more of the pixels (Col. 11, lines 3 – 40). Fossum (Fig. 8) shows how a block of 3 x 3 would be processed through the averaging circuit (608 and 610) (Col. 11, lines 23 – 32). Fossum also teaches the multi-resolution readout architecture can be set by programmable switches (Col. 12, lines 14 - 20). The microprocessor of Voss and the programmable switches of Fossum could be the same unit. When the quantity of incident light is larger than a predetermined higher reference quantity that is larger, than the reference quantity, an output of the averaging portion is read out to the signal line in place of the added signal (Col. 11, lines 3 – 40). Fossum (Fig. 8) shows how a block of 3 x 3 would be processed through the averaging circuit (608 and 610) (Col. 11, lines 23 – 32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided averaging pixel signals as taught by Fossum to the imaging sensor device of Parrish in view of Voss, because block averaging process produces a lower resolution image, reduces processing time, enhances the output signal, and allows low light imaging (Col. 4, lines 22 – 55 of Fossum).

As to claims 15, this claim differs from claim 8 only in that the claim 15 depends on claim 2 and claim 8 depends on claim 1. Thus claim 15 is analyzed as previously discussed with respect to claims 8 above.

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (US Patent # 6,593,562) in view of Voss (US Patent # 7,233,354) as applied to claims 3 and 4 above, and further in view of Takayama (US Patent # 7,088,395).

As to claim 6, note the discussion of Voss in view of Fossum above, Voss in view of Fossum do not teach a photometer portion is provided between the imaging region and the signal line so as to detect a quantity of the incident light onto the imaging region. Takayama teaches a photometer portion (150b) is provided between the imaging region (54) and the signal line (w1 and w2) so as to detect a quantity of the incident light onto the imaging region (54). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a photometer portion is provided between the imaging region and the signal line so as to detect a quantity of the incident light onto the imaging region as taught by Takayama to the image capturing device of Voss in view of Fossum, because the image-capturing apparatus will reduce its power consumption, low-cost and reduce the number of necessary parts (Col. 2, line 62 – Col. 3, line 10 of Takayama).

As to claim 7, claim 7 cites a photometer portion is arranged between the two or more pixels as to claim 6. Takayama teaches a photometer portion (50b in Fig. 4) is arranged between the two or more pixels (50a).

7. Claims 21 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (US Patent # 6,593,562) in view of Voss (US Patent # 7,233,354) as applied to claims 1 and 2 above, and further in view of Sharma (US Patent Pub. # 2004/0008542).

As to claim 21, Voss in view of Fossum teach a storage portion. Voss in view of Fossum do not specifically teach a storage portion composed of a capacitor. Sharma teaches a memory backup system. The memory back-up system includes a first memory cell, and a non-volatile memory cell that is interfaced to the first memory cell. Control circuitry allows data to be written to either the first memory cell or the non-volatile memory cell, and provides transfer of the data from either the first memory cell or the non-volatile memory cell, to the other of either the first memory cell or the non-volatile memory cell. Sharma (Fig. 3) teaches the storage portion (DRAM / MRAM memory cell 300) is composed of a capacitor (CD) (Para 28 and 29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a DRAM / MRAM memory cell as taught by Sharma to the image capturing device of Voss in view of Fossum, because the memory system allows for efficient transfer of large amounts of data between the volatile and non-volatile memory (Para 14 of Sharma).

As to claim 22, this claim differs from claim 21 only in that the claim 22 depends on claim 2 whereas claim 21 depends on claim 1. Thus method claim 22 is analyzed as previously discussed with respect to claim 21 above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **CHRISTOPHER K. PETERSON** whose telephone number is (571)270-1704. The examiner can normally be reached on Monday - Friday 6:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran Sinh can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. K. P./
Examiner, Art Unit 2622
5 Dec 2008

/Sinh N Tran/
Supervisory Patent Examiner, Art Unit 2622